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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,764	04/02/2004	Cyrus E. Tabery	H1779	2770

61060 7590 01/30/2007
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EXAMINER	
LEVIN, NAUM B	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,764	TABERY ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *17-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 11-16* is/are rejected.

7)☒ Claim(s) *2,3 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/816,764, Response to Election/Restriction filed on 11/03/2006, and Amendment filed on 08/22/2006. Applicants have elected claims 1-16 (Group 1) without traverse. Claims 17-24 have been withdrawn from consideration.

2. The Examiner finds Applicant's arguments on the applications of Maurer as none persuasive. Maurer's reference reads on the claims 1, 4-7 and 11-16 as presently written.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-7 and 11-16 are rejected under 35 U.S.C. 102(e) as being unpatentable by Maurer et al. (US Pub. No.: 2004/0063000).

3. As to claim 1 Maurer discloses:

(1) A method of manufacturing an integrated circuit (IC) device having a given layout, said method comprising:

simulating how structures (FIG. 5A shows mask error function (MEF) and critical dimension on a wafer as a function of critical dimension on a mask obtained by

simulations based on chromeless-phase lithography (CPL)- [0031]; pattern transfer can be configured based on RETs such as alt-PSM, DDL, and CPL, or other techniques - [0060]) within the layout (A computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs [0046]) will pattern on a wafer (Integrated circuit patterns are typically transferred from a pattern mask or reticle to a substrate ... The substrate is generally a wafer of silicon or other semiconductor material – [0044]) for a plurality of resolution enhancement techniques (RETs) (FIG. 5A includes a curve 502 representing mask error factor (MEF) as a function of critical dimension on a mask. MEF is defined as a ratio of a change in a CD on a wafer to a corresponding change in a CD on a mask [0062]) ([0031]; [0044]; [0046]; [0060]; [0062]);

evaluating manufacturability of structures within each simulation (a tool can be configured ... to provide an indication of a simulated performance of a selected RET with respect to other available (or unavailable) RETs. Because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated, and mask designs based on a selected process can be verified prior to mask fabrication –[0046]) ([0045]- [0046]; [0052]; [0075]); and

selecting one or more RETS that provide optimal manufacturability (A computer-based design tool can be configured to access layout data stored in a database and ... select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. For example, such a tool can be

configured to select a preferred RET for a particular pattern feature, or to provide an indication of a simulated performance of a selected RET with respect to other available (or unavailable) RETs ... and mask designs based on a selected process can be verified prior to mask fabrication – [0046]; DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch – [0050]; Using the MEF curve 502, features sizes in a particular design can be identified as small, intermediate, or large based on the sign of the MEF and an appropriate technique used to define corresponding portions of a mask. For example, as noted above, pattern transfer of features of intermediate size can be implemented in CPL with SRAFs. Large features can be defined using a series of alternating phase stripes (alt-PSM) of constant or variable pitch, using opaque chromium, or otherwise defined. A particular phase-edge arrangement can be selected based on a selected process window for one or more pattern features. Alternatively, a phase-edge density can be selected based on a feature size, so that a fixed or variable number of phase edges are used to define the feature – [0062]) ([0046]; [0048]- [0050]; [0062]);

4. As to claims 4-7 and 11-16 Maurer recites:

(4), (6), (12), (13) The method, wherein each RET includes a combination of illuminator parameters, numerical aperture (NA) and mask parameters ([0003]; [0049]; [0050]; [0060]);

(5) The method, wherein the illuminator parameters include at least one of illuminator source shape, number of poles, orientation of poles, inner radius, outer radius, and wedge angle ([0049]);

(7) The method, wherein the simulating step includes simulating variations ([0032]; claim 41);

(11) The method further comprising based on the simulating step, providing a graphical representation ([0071]-[0072]);

(14), (15), (16) The method, wherein the same simulation engine is used to perform OPC and RETs simulation ([0072]-[0074]).

REMARKS

5. Mostly Applicant argues: "Maurer does not disclose evaluating manufacturability of structures within each simulation".

First of all, the terminology of claim 1 should be explained in view of Applicants Specification. Specification recites: "each simulation image can be examined to determine whether it includes areas, regions or features (e.g., structure edges), which demonstrate or are otherwise indicative of poor or acceptable manufacturability for a given RET- paragraph 36 ... Regions, features or edges demonstrating or exhibiting poor manufacturability can be determined or otherwise identified by applying one or more optical rule checking (ORC) - paragraph 37".

Maurer, for example disclose: "FIGS. 1A-1B are graphs of normalized image log slopes (NILS) as a function of defocus that illustrate the performance of alt-PSM, DDL, and CPL for an isolated 65 nm wide line (FIG. 1A) and nested 65 nm lines at a 160 nm pitch (FIG. 1B). Normalized image log slope is defined as NILS = dlnI/dlnx/edge, wherein I=relative aerial image intensity and x=wafer coordinate. ... As shown in FIGS. 1A-1B, both DDL and CPL exhibit performance comparable to alt-PSM. The graphs of

FIGS. 1A-1B are based on simulations of aerial image intensities, i.e., on simulated radiation intensities at a wafer surface as a function of location on the wafer surface – paragraph 52".

Maurer, for example discloses: "the ORC tool 712 can be configured to identify design areas having potentially unacceptable device performance and/or process yield. Typically the ORC tool 712 compares predicted manufacturing results with an IC design based on a calculation of edge placement error (EPE). Large EPEs typically indicate problem areas – paragraph 75".

6. Next Applicant argues: "Maurer does not disclose selecting one or more RETS that provide optimal manufacturability".

Maurer, e.g. teaches: "A computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. For example, such a tool can be configured to select a preferred RET for a particular pattern feature – paragraph 46; one RET is based on alternating phase-shift masks (alt-PSMs) ... Alt-PSMs can be used to achieve effective resolutions of k.sub.1.ltoreq.0.3, and manufacture of such masks can be straightforward - paragraph 48; other RETs such as double-exposure dipole lithography (DDL) use off-axis mask illumination. Pattern-transfer with such RETs typically exhibits resolution dependences on off-axis illumination directions. For example, in DDL, pattern transfer of dense lines and spaces oriented with respect to a selected axis exhibits the same effective resolution as alt-PSM - paragraph 49".

7. Also Applicant argues: "Maurer does not disclose "wherein each RET includes a combination of illuminator parameters, numerical aperture (NA) and mask parameters" as recited in claim 4".

Maurer, e.g. describes: "the effective resolution of lithographic systems can be increased by applying one or more so-called resolution enhancement techniques (RETs). Such increases in effective resolution can be associated with a parameter k1=CD/lambda/NA, wherein CD is a critical dimension associated with a particular set of design rules – paragraph 4".

8. Further Applicant argues: "Maurer does not disclose "wherein the illuminator parameters include at least one of illuminator source shape, number of poles, orientation of poles, inner radius, outer radius, and wedge angle" as recited in claim 5".

Maurer, e.g., recites: "Other RETs such as double-exposure dipole lithography (DDL) use off-axis mask illumination – paragraph 49".

9. Next Applicant argues: "Maurer does not disclose "wherein the mask parameters include at least one of mask type and mask transmission" as recited in claim 6".

Maurer, e.g., discloses: "The following Table summarizes some features of available RETs and combinations, including simple OPC and high-transmission attenuated phase-shift masks (HT-PSM), i.e. phase shift masks that include regions having transmissions as low as about 5% to 15% - paragraph 60 ".

10. Applicant also argues: "Maurer does not disclose "wherein the simulating step includes simulating variations over a predetermined range in at lest one of focus, exposure and the mask" as recited in claim 7".

Maurer, e.g., recites: "A method of selecting size ranges for CPL mask definition, comprising: simulating aerial intensities for a plurality of isolated features having respective feature widths; and establishing a minimum feature size range based on a feature size associated with a minimum aerial intensity – claim 41 ".

Allowable Subject Matter

11. Claims 2-3 and 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A method of manufacturing an integrated circuit (IC) device having a given layout, said method comprising:

simulating how structures within the layout will pattern on a wafer for a plurality of resolution enhancement techniques (RETs);

evaluating manufacturability of structures within each simulation; and

selecting one or more RETS that provide optimal manufacturability,

wherein the evaluating step includes:

performing optical rule checking (ORC) on structures within each simulation; and

calculating a percentage of optically different edges that demonstrate acceptable manufacturability, and

wherein the electing step includes selecting RETs that correspond to simulations having a percentage of acceptable optically different edgesw that is greater than a predefined value.

12. As to claims 1, 4-7 and 11-16 Examiner defined Applicant's arguments as none persuasive.

13. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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VUTHE SIEK
PRIMARY EXAMINER